IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001] The present invention relates generally to methods and structures for stabilizing a semiconductor device, such as a flip-chip type semiconductor die or a chip scale package (CSP), when disposed in ~~face-down~~ face-down orientation over a carrier substrate, such as a circuit board. The stabilizer structures of the present invention are also useful for spacing a semiconductor device a substantially uniform desired distance away from the carrier substrate. More specifically, the invention pertains to stereolithographically fabricated stabilizers and to the use of stereolithographic methods to fabricate the stabilizers.

Please amend paragraph number **[0002]** as follows:

[0002] Flip-chip technology, including chip scale packaging technology, is widely used in the electronics industry. In both the generic flip-chip and the chip scale packaging technologies, a semiconductor device having a pattern of conductive pads on an active surface thereof is joined face down to a ~~higher level~~ higher-level substrate, such as a printed circuit board. The contact pads of the ~~higher level~~ higher-level substrate are arranged in a mirror image to corresponding contact pads on the semiconductor device. Conductive structures, typically solder bumps (as exemplified by the so-called C-4 technology), conductive epoxy bumps or pillars, conductor-filled epoxy, or an anisotropically conductive z-axis elastomer, join contact pads on the surface of the semiconductor device with their corresponding contact pads on the ~~higher level~~ higher-level substrate, establishing electrical communication between the semiconductor device and the ~~higher level~~ higher-level substrate.

Please amend paragraph number **[0003]** as follows:

[0003] When the semiconductor device is a flip-chip type semiconductor die, the spacing or pitch between adjacent contact pads, or bond pads, is relatively small. The contact pads themselves are also very small. State of the art flip-chip type semiconductor dice typically include many contact pads in an array on the active surfaces thereof. The high density, small

feature size, and large number of conductive pads on state of the art semiconductor dice make the disposal of uniformly sized and configured conductive structures thereon a challenging process. Relatively small variations in the size or shape of the conductive structures can be accommodated during bonding of the conductive structures to the contact pads of the ~~higher level~~ higher-level substrate. However, due to larger dimensional variations in the conductive structures on flip-chip type semiconductor dice, higher bonding temperatures or compressive forces are typically required to ensure the formation of adequate bonds between the bond pads of a flip-chip type semiconductor die and the corresponding contact pads of a ~~higher level~~ higher-level substrate. The use of higher temperatures can damage the circuitry and other features of the semiconductor die, as well as impair the integrity of the conductive structures. Overcompression of the conductive structures can also be detrimental. When a compressed conductive structure spreads over and contacts the glass (e.g., borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), or borosilicate glass (BSG)) passivation layer that typically surrounds the bond pads of a semiconductor die, thermal cycling of the semiconductor die during subsequent processing or in use can fracture the conductive structure and diminish the electrical conductivity thereof.

Please amend paragraph number **[0005]** as follows:

[0005] Moreover, some semiconductor dice have bond pads that are positioned in locations that will not adequately and stably support these dice when conductive structures are secured thereto and the dice are disposed face down (i.e., in a flip-chip orientation) over a ~~higher level~~ higher-level substrate. Examples of such dice include leads over chip (LOC)-configured semiconductor dice and semiconductor dice with one or two rows of bond pads along the central axes of the dice with bond pads positioned adjacent only a single peripheral edge thereof. Thus, when conductive structures are secured to the bond pads of such a semiconductor die and the semiconductor die is then positioned face down relative to a ~~higher level~~ higher-level substrate, the die is prone to being tipped or tilted from an intended orientation that is substantially parallel to a plane of the contact ~~pad~~

~~bearing~~ pad-bearing surface of the ~~higher level~~ higher-level substrate. As a consequence, such dice are thought to be unsuitable for flip-chip applications without rerouting of the bond pads to a more stable arrangement. In addition, one or two rows of bond pads bearing solder bumps may not exhibit sufficient surface tension during reflow of the solder to support the die, resulting in collapse or flattening of the masses of molten solder and shorts of adjacent connections. Inadequate support strength may also be a problem with other materials.

Please amend paragraph number **[0007]** as follows:

[0007] FIG. 1 illustrates an LOC-configured semiconductor die 200 having two centrally located rows of bond pads 202 on an active surface 204 thereof. The two rows of bond pads 202 are located between opposite side edges 226 and 228 of die 200 and extend generally parallel to side edges 226 and 228. Die 200 can be flip-chip connected to a ~~higher level~~ higher-level substrate, in this case a carrier substrate 210. Carrier substrate has contact pads 230 exposed at a surface 214 thereof. When die 200 is assembled with carrier substrate 210 in a flip-chip type arrangement, as shown in FIG. 2, die 200 is to be inverted relative to carrier substrate 210, with bond pads 202 being aligned with their corresponding contact pads 230.

Please amend paragraph number **[0015]** as follows:

[0015] Thus, it is apparent that a need exists for a method and apparatus for adequately stabilizing a semiconductor device, such as a semiconductor die or chip scale package bearing few conductive structures and/or bearing conductive structures in an inherently unstable arrangement, when disposed face down over a ~~higher level~~ higher-level substrate, such as a carrier substrate. There is also a need for a method and structure that facilitate spacing a semiconductor device face down over a ~~higher level~~ higher-level substrate a substantially uniform distance and that facilitate the maintenance of conductive structures in desired shapes and dimensions following the connection of the semiconductor device to the ~~higher level~~ higher-level substrate by way of the conductive structures.

Please amend paragraph number **[0016]** as follows:

[0016] In the past decade, a manufacturing technique termed ~~"stereolithography",~~ "stereolithography," also known as "layered ~~manufacturing",~~ manufacturing," has evolved to a degree where it is employed in many industries.

Please amend paragraph number **[0022]** as follows:

[0022] The present invention includes stabilizers, which are also referred to herein as spacers, as support structures, or as outriggers, that are positionable on a surface of a semiconductor device, such as on the active surface of a semiconductor die to be disposed face down through use of projecting conductive structures over a ~~higher level~~ higher-level substrate, as on the surface of a chip scale package from which conductive structures protrude. The stabilizers of the present invention may be used with semiconductor devices having bond pads arranged in such a manner that conductive structures, or elements, secured thereto will not adequately support the semiconductor device when disposed face down on a ~~higher level~~ higher-level substrate.

Please amend paragraph number **[0023]** as follows:

[0023] Stabilizers incorporating teachings of the present invention are configured and located to, along with conductive structures, stabilize a semiconductor device when disposed face down over a ~~higher level~~ higher-level substrate.

Please amend paragraph number **[0024]** as follows:

[0024] The stabilizers of the present invention may also be configured to maintain a substantially parallel relation between a carrier substrate and a semiconductor device to be disposed in a ~~face down~~ face-down orientation over the carrier substrate. Stabilizers are also configured to space the semiconductor device and the carrier substrate a minimum distance apart from one another during and after the electrical connection of contact pads of the semiconductor device to corresponding contact pads of the carrier substrate. The stabilizers are configured to

support the semiconductor device in spaced apart relation on the carrier substrate before, during, and after electrical connections are established between the semiconductor device and the carrier substrate.

Please amend paragraph number **[0040]** as follows:

[0040] FIG. 5 is a cross-sectional view of an assembly including another semiconductor device disposed on a substrate in ~~a face down~~ face-down orientation, with the semiconductor device being tipped or tilted relative to the substrate;

Please amend paragraph number **[0043]** as follows:

[0043] FIG. 8 is an enlarged partial perspective assembly view of a semiconductor device having stabilizers on a surface thereof, the semiconductor device being disposed on a substrate in ~~a face down~~ face-down orientation;

Please amend paragraph number **[0044]** as follows:

[0044] FIG. 9 is a cross-sectional view of an assembly with a semiconductor device disposed on a substrate in ~~a face down~~ face-down orientation, the semiconductor device including stabilizers to separate the surface of the semiconductor device a substantially uniform distance from the surface of the substrate;

Please amend paragraph number **[0052]** as follows:

[0052] As depicted in FIG. 8, semiconductor device 10 has four stabilizers 50 protruding from an active surface 14 thereof. Stabilizers 50, which are also referred to herein as support structures, spacers, or outriggers, preferably protrude substantially equal distances from active surface 14 to a common plane. Stabilizers 50 are preferably configured and located so as to at least partially horizontally stabilize semiconductor device 10 when disposed ~~face down~~ face down over ~~a higher level~~ higher-level substrate, such as substrate 20. Stabilizers 50 may be

configured and positioned on semiconductor device 10 to horizontally stabilize semiconductor device 10 in combination with any conductive structures protruding therefrom.

Please amend paragraph number **[0058]** as follows:

[0058] If the conductive material of the conductive structures, such as solder bumps 30, will sag when reflowed, stabilizers 50 may protrude from active surface 14 a greater distance 54 than the distance 60 that conductive structures, such as solder bumps 30, protrude from active surface 14. Such sagging of the conductive material during reflow facilitates the formation of electrical connections between bond pads 12 and contact pads 40 even when ~~spacers~~ stabilizers 50 are taller than the conductive structures. Thus, the use of taller ~~spacers~~ stabilizers 50 may facilitate the formation of taller, thinner conductive structures.

Please amend paragraph number **[0077]** as follows:

[0077] Apparatus 80 also includes a reservoir 84 (which may comprise a removable reservoir interchangeable with others containing different materials) of liquid material 86 to be employed in fabricating the intended object. In the currently preferred embodiment, the liquid is a photo-curable polymer, or ~~"photopolymer",~~ "photopolymer," that cures in response to light in the UV wavelength range. The surface level 88 of material 86 is automatically maintained at an extremely precise, constant magnitude by devices known in the art responsive to output of sensors within apparatus 80 and preferably under control of computer 82. A support platform or elevator 90, precisely vertically movable in fine, repeatable increments responsive to control of computer 82, is located for movement downward into and upward out of material 86 in reservoir 84.

Please amend paragraph number **[0080]** as follows:

[0080] Referring now to FIGs. 20 and 21, data from the STL files resident in computer 82 is manipulated to build an object, such as stabilizers ~~50~~ 50, illustrated in FIGs. 8-19 and ~~22~~ 22, or base supports 122, one layer at a time. Accordingly, the data mathematically representing one

or more of the objects to be fabricated are divided into subsets, each subset representing a slice or layer of the object. The division of data is effected by mathematically sectioning the 3-D CAD model into at least one layer, a single layer or a "stack" of such layers representing the object. Each slice may be from about 0.0001 to about 0.0300 inch thick. As mentioned previously, a thinner slice promotes higher resolution by enabling better reproduction of fine, vertical surface features of the object or objects to be fabricated.

Please amend paragraph number **[0082]** as follows:

[0082] Before fabrication of a first layer for a support 122 or an object to be fabricated is commenced, the operational parameters for apparatus 80 are set to adjust the size (diameter if circular) of the laser light beam used to cure material 86. In addition, computer 82 automatically checks and, if necessary, adjusts by means known in the art, the surface level 88 of material 86 in reservoir 84 to maintain same at an appropriate focal length for laser beam 98. U.S. Patent No. 5,174,931, referenced above and previously incorporated herein by reference, discloses one suitable level control system. Alternatively, the height of mirror 94 may be adjusted responsive to a detected surface level 88 to cause the focal point 148 of laser beam 98 to be located precisely at the surface of material 86 at surface level 88 if level 88 is permitted to vary, although this approach is more complex. Platform 90 may then be submerged in material 86 in reservoir 84 to a depth equal to the thickness of one layer or slice of the object to be formed, and the liquid surface level 88 is readjusted as required to accommodate material 86 displaced by submergence of platform 90. Laser 92 is then activated so laser beam 98 will scan unconsolidated (e.g., liquid or powdered) material 86 disposed over surface 100 of platform 90 to at least partially consolidate (e.g., polymerize to at least a semisolid state) material 86 at selected locations, defining the boundaries of a first layer 122A of base support 122 and filling in solid portions thereof. Platform 90 is then lowered by a distance equal to thickness of second layer 122B, and laser beam 98 scanned to define and fill in the second layer while simultaneously bonding the second layer to the first. The process may be then repeated, as often as necessary, layer by layer, until base support 122 is completed. Platform 90 is then moved relative to the mirror 94 to form

any additional base supports 122 on platform 90 or a substrate disposed thereon or to fabricate objects upon platform 90, base support 122, or a substrate, as provided in the control software. The number of layers required to erect support 122 or other objects to be formed depends upon the height of the object to be formed and the desired layer thickness 108, 110. The layers of a stereolithographically fabricated structure with a plurality of layers may have different thicknesses.

Please amend paragraph number **[0085]** as follows:

[0085] Yet another alternative to layer preparation of unconsolidated (e.g., liquid) material 86 is to merely lower platform 90 to a depth 87 equal to that of a layer of material 86 to be scanned, and to then traverse a combination flood bar and meniscus bar assembly horizontally over platform 90, a substrate disposed on platform 90, or one or more objects being formed to substantially concurrently flood material 86 thereover and to define a precise layer thickness of material 86 for scanning.

Please amend paragraph number **[0087]** as follows:

[0087] In practicing the present invention, a commercially available stereolithography apparatus operating generally in the manner as that described above with respect to apparatus 80 of FIG. 20 is preferably employed, but with further additions and modifications as hereinafter described for practicing the method of the present invention. For example and not by way of limitation, the SLA-250/50HR, SLA-5000 and SLA-7000 stereolithography systems, each offered by 3D Systems, Inc. of Valencia, California, are suitable for modification. Photopolymers believed to be suitable for use in practicing the present invention include Cibatool SL 5170 and SL 5210 resins for the SLA-250/50HR system, Cibatool SL 5530 resin for the SLA-5000 and 7000 systems, and Cibatool SL 7510 resin for the SLA-7000 system. All of these photopolymers are available from Ciba Specialty Chemicals ~~Corporation.~~ Inc.

Please amend paragraph number **[0088]** as follows:

[0088] By way of example and not limitation, the layer thickness of material 86 to be formed, for purposes of the invention, may be on the order of about 0.0001 to 0.0300 inch, with a high degree of uniformity. It should be noted that different material layers may have different heights, so as to form a structure of a precise, intended total height or to provide different material thicknesses for different portions of the structure. The size of the laser beam "spot" or focal point 148 impinging on the surface of material 86 to cure same may be on the order of 0.001 inch to 0.008 inch. Resolution is preferably ±0.0003 inch in the X-Y plane (parallel to surface 100) over at least a 0.5 inch × 0.25 inch field from a center point, permitting a high resolution scan effectively across a 1.0 inch × 0.5 inch area. Of course, it is desirable to have substantially this high a resolution across the entirety of surface 100 of platform 90 to be scanned by laser beam 98, such area being termed the "field of ~~exposure",~~ exposure," such area being substantially coextensive with the vision field of a machine vision system employed in the apparatus of the invention as explained in more detail below. The longer and more effectively vertical the path of laser beam 96/98, the greater the achievable resolution.

Please amend paragraph number **[0094]** as follows:

[0094] Continuing with reference to FIGs. 20 and 21, the semiconductor device or devices 10 on platform 90 may then be submerged partially below the surface level 88 of liquid material 86 to a depth greater than the thickness of a first layer of material 86 to be at least partially consolidated (e.g., cured to at least a semisolid state) to form the lowest layer 130 of each stabilizer 50 at the appropriate location or locations on each semiconductor device 10, then raised to a depth equal to the layer thickness, surface level 88 of material 86 being allowed to become calm. Photopolymers that are useful as material 86 exhibit a desirable dielectric constant, low shrinkage upon cure, are of sufficient (i.e., semiconductor grade) purity, exhibit good adherence to other semiconductor device materials, and have a sufficiently similar coefficient of thermal expansion (CTE) to the material of the conductive structures (e.g., solder or other metal or metal alloy). As used herein, the term "solder ball" may also be interpreted to

encompass conductive or conductor filled epoxy. Preferably, the CTE of material 86 is sufficiently similar to that of the conductive structures to prevent undue stressing of the conductive structures or of semiconductor device 10 during thermal cycling thereof in testing and subsequent normal operation. One area of particular concern in determining resin suitability is the substantial absence of mobile ions and, specifically, of fluoride ions. Exemplary photopolymers exhibiting these properties are believed to include, but are not limited to, the above-referenced resins from Ciba Specialty ~~Chemical Company.~~ Chemicals Inc.

Please amend paragraph number **[0104]** as follows:

[0104] While a variety of methods may be used to fabricate stabilizers 50, the use of a stereolithographic process as exemplified above is a preferred method because a large number of stabilizers 50 may be fabricated in a short time, the stabilizer height and position are ~~computer-controlled~~ computer-controlled to be extremely precise, wastage of unconsolidated material 86 is minimal, solder coverage of passivation materials is reliably avoided through precise spacer height control, and the stereolithography method requires less handling of semiconductor devices 10 or other substrates than the other viable methods indicated above.